St. Thomas College of Engineering & Technology
Vellilode, Sivapuram PO. Mattanur. Kannur District, Kerala
Approved by AICTE New Delhi, Govt. Of Kerala and Affiliated to APJ Abdul Kalam Technological University

COURSE HANDOUT

(B. Tech - Semester 3)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COLLEGE VISION

To be an Institute of repute recognized for excellence in education, innovation, and social contribution.

COLLEGE MISSION

M1: Infrastructural Relevance - Develop, maintain and manage our campus for our stakeholders.
M2: Life-Long Learning - Encourage our stakeholders to participate in lifelong learning through industry and academic interactions.
M3: Social Connect - Organize socially relevant outreach programs for the benefit of humanity.

DEPARTMENT VISION

To produce professionally competent, ethically sound and socially responsible Electronics and Communication Engineers.

DEPARTMENT MISSION

M1: Provide excellent infrastructure and lab facilities for quality education.

M2: Promote industry-academic interactions to keep up with technological advancements.

M3: Develop interpersonal skills and social responsibility among students through project-based and team-based learning.

PROGRAM EDUCATIONAL OBJECTIVES (PEO)

Graduates of B. Tech ECE program after graduation will:

PEO1: Exemplify technical competence in designing, analyzing, testing and fabricating electronic circuits.

PEO2: Acquire leadership qualities, rapport, communication skills in the organization and adapt to changing professional and societal needs.

PEO3: Work effectively as individuals and as team members in multidisciplinary projects

PROGRAM OUTCOMES (POS)

Engineering Graduates will be able to:

PO1 Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2 Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3 Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4 Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5 Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6 The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7 Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8 Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9 Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10 Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11 Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12 Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSO)

PSO1: Define, design, implement, model, and test electronic circuits and systems that perform signal processing functions.

PSO2: Segregate and select appropriate technologies for implementation of a modern communication system.

CONTENTS

COURSE INFORMATION SHEETS OF SEMESTER 3 COURSES

COURSE CODE	COURSE NAME
GYMAT301	MATHEMATICS FOR ELECTRICAL/PHYSICAL SCIENCE-3
PCECT302	SOLID STATE DEVICES
PCECT303	ANALOG CIRCUITS
PBECT304	LOGIC CIRCUIT DESIGN (PROJECT-BASED LEARNING)
GNEST305	INTRODUCTION TO ARTIFICIAL INTELLIGENCE AND DATA SCIENCE
UCHUT347	ENGINEERING ETHICS AND SUSTAINABLE DEVELOPMENT
PCECL307	ANALOG CIRCUITS LAB
PCECL308	LOGIC CIRCUIT DESIGN LAB

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PCECL308

LOGIC CIRCUIT DESIGN LAB

COURSE INFORMATION SHEET

PROGRAMME: ECE (UG)	**DEGREE**: BTECH
COURSE: LOGIC CIRCUIT DESIGN LAB	**SEMESTER: III** **L-T-P-R 0:0:3:0 CREDITS**: 2
COURSE CODE: PCECL308 **REGULATION**:2024	**COURSE TYPE**: LAB
COURSE AREA/DOMAIN: DIGITAL ELCTRONICS	**CONTACT HOURS**:3 HRS/WEEK
CORRESPONDING LAB COURSE CODE (IF ANY):	**LAB COURSE NAME**:

SYLLABUS

EXPERIMENT NO:	EXPERIMENTS	HOURS
	Part A – List of Experiments using digital components (Any Six experiments mandatory)	
1	Realization of functions using basic and universal gates (SOP and POS forms).	3
2	Design and Realization of half/full adder and subtractor using basic gates and universal gates.	3
3	4-bit adder/subtractor and BCD adder using 7483	3
4	Study of Flip Flops: S-R, D, T, JK and Master slave JK FF using NAND gates	3
5	Asynchronous Counter: 3 bit up/down counter, Realization of Mod N Counter	3
6	Synchronous Counter: Realization of 4-bit up/down counter, Realization of Mod-N counters	3
7	Ring counter and Johnson Counter.	3
8	Realization of counters using IC's (7490, 7492, 7493).	3
9	Realization of combinational circuits using MUX & DEMUX, using ICs (74150, 74154)	3
10	Sequence Generator / Detector	3
	Part B – Simulation Experiments (Any Six experiments mandatory)	

1	Experiment 1: Realization of Logic Gates and Familiarization of FPGAs (a) Familiarization of a small FPGA board and its ports and interface. (b) Create the .pcf files for your FPGA board. (c) Familiarization of the basic syntax of Verilog Development of Verilog modules for basic gates, synthesis and implementation in the above FPGA to verify the truth tables. (e) Verify the universality and non-associativity of NAND and NOR gates by uploading the corresponding Verilog files to the FPGA boards.	3
2	Experiment 2: Adders in Verilog (a) Development of Verilog modules for half adder in any of the 3 modeling styles (b) Development of Verilog modules for full adder in structural modeling using half adder	3
3	Experiment 3: Mux and Demux in Verilog (a) Development of verilog modules for a 4x1 MUX. (b) Development of Verilog modules for a 1x4 DEMUX.	3
4	Experiment 4: Flipflops and counters (a) Development of Verilog modules for SR, JK and D flipflops. (b) Development of Verilog modules for a binary decade/Johnson/Ring counter	3
5	Experiment 5. Multiplexer and Logic Implementation in FPGA (a) Make a gate level design of an 8 : 1 multiplexer, write to FPGA and test its functionality. (b) Use the above module to realize any logic function	3
6	Experiment 6. Flip-Flops and their Conversion in FPGA (a) Make gate level designs of J-K, J-K master-slave, T and D flip-flops, implement and test them on the FPGA board. (b) Implement and test the conversions such as T to D, D to T, J-K to T and J-K to D	3
7	Experiment 7: Asynchronous and Synchronous Counters in FPGA (a) Make a design of a 4-bit up down ripple counter using T-flip-flops in the previous experiment, implement	3

	and test them on the FPGA board. (b) Make a design of a 4-bit up down synchronous counter using T-flip-lops in the previous experiment, implement and test them on the FPGA board	
8	Experiment 8: Universal Shift Register in FPGA (a) Make a design of a 4-bit universal shift register using D-flip-flops in the previous experiment, implement and test them on the FPGA board. (b) Implement ring and Johnson counters with it.	3
9	Experiment 9. BCD to Seven Segment Decoder in FPGA (a) Make a gate level design of a seven-segment decoder, write to FPGA and test its functionality. (b) Test it with switches and seven segment display. Use output ports for connection to the display.	3
Total hours		57

TEXT BOOKS/REFERENCE BOOKS:

T/R	BOOK TITLE/AUTHORS/PUBLICATION
T1	Verilog HDL Synthesis: A Practical Primer J. Bhasker B. S. Publications, 2001
T2	Fundamentals of Logic Design Roth C.H Jaico Publishers. V Ed., 2009 5th Edition
R1	Verilog HDL :A guide to digital design and synthesis Palnitkar S. Prentice Hall; 2003. 2nd Edn.

COURSE PREREQUISITES: NIL

COURSE OBJECTIVES:

1	Familiarise the students with the Digital Logic Design through the implementation of Logic Circuits.
2	Familiarise the students with the HDL based Digital Design and FPGA boards

COURSE OUTCOMES:

After the completion of the course, the student will be able to

COs / CO-PO/PSO MAPPING. /BLOOM'S TAXONOMY LEVEL	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
PCECL308.1	Design and demonstrate the functioning of various combinational and sequential circuits using ICs.													
	3	**3**	**3**	**2**					**3**			**3**	**3**	**2**
	APPLY													
PCECL308.2	Apply an industry compatible hardware description language to implement digital circuits													
	3	**1**	**1**	**3**	**3**				**3**	1		**3**	**3**	**2**
	APPLY													
PCECL308.3	Implement digital circuits on FPGA boards and connect external hardware to the board													
	3	**1**	**1**	**3**	**3**				**3**	**1**		**3**	**3**	**2**
	APPLY													
PCECL308.4	Function effectively as an individual and in a team to accomplish the given task.													
	3	**3**	**3**		**3**				**3**			**3**	**1**	**1**
	APPLY													
MAPPING AVERAGE	3	2.00	2.00	2.67	3.00				3.00	1		3	2.5	1.75

JUSTIFICATION FOR CO-PO/PSO MAPPING:

CO	PO/PSO	MAPPING LEVEL	JUSTIFICATION
PCECL308.1	PO1	3	Strongly involves applying fundamental concepts of digital electronics and logic design.
	PO2	3	Requires analysis of circuit functionality and behavior to design correct combinational and sequential logic circuits.
	PO3	3	Focus is on designing and demonstrating digital

			solutions using ICs—directly addresses this PO.
	PO4	2	Involves experimentation, testing circuits for correctness, and interpreting results to verify performance.
	PO9	3	Students typically work in teams for lab-based tasks, promoting collaboration while also requiring individual contributions.
	PO12	3	Encourages learning of evolving digital ICs and technologies beyond classroom theory, a key component of lifelong learning
	PSO1	3	The CO involves **designing and demonstrating circuits** (both combinational and sequential), which directly supports **design, implementation, and testing** of electronic circuits as mentioned in PSO1.
	PSO2	2	The CO has an **indirect link** to communication systems, as basic combinational/sequential circuits are **building blocks** in communication system design, but the CO does not explicitly address communication applications.
PCECL308.2	PO1	3	Requires foundational knowledge of digital electronics and hardware description languages (HDL) to implement functional digital systems.
	PO2	1	Involves limited problem analysis; focus is more on translating known designs into HDL rather than exploring or analyzing open-ended problems.
	PO3	1	While it includes design using HDL, the design complexity may be minimal or already defined, hence low emphasis.
	PO4	3	Includes simulation, verification, and debugging of HDL-based designs—key aspects of investigation and evaluation.

	PO5	3	Strong use of modern industry-relevant tools (e.g., Xilinx Vivado, ModelSim, Quartus) for design, simulation, and implementation.
	PO9	3	Students work individually and in groups during lab activities, encouraging collaboration and independent problem solving.
	PO10	1	May involve minimal reporting or explanation of HDL code; however, formal communication (e.g., documentation or presentation) is not the primary focus.
	PO12	3	Working with HDL promotes self-learning of industry-relevant tools and languages, fostering continuous skill development aligned with industry trends.
	PSO1	3	HDL implementation of digital circuits directly relates to design, modeling, and implementation of electronic circuits, which are core to PSO1.
	PSO2	2	Using HDL can be part of selecting appropriate technologies for modern communication systems, though the CO does not explicitly focus on communication.
PCECL308.3	PO1	3	Involves core knowledge of digital logic, circuit interfacing, and FPGA architecture to implement functional systems.
	PO2	1	Problem-solving is limited to predefined hardware interfacing tasks; not focused on deep analytical problem resolution.
	PO3	1	Although design is part of the implementation, the task may involve replicating existing designs rather than creating new solutions.
	PO4	3	Debugging, testing, and validating FPGA outputs with connected hardware requires systematic investigation and analysis.

	PO5	3	Strong exposure to industry-relevant tools like Xilinx Vivado/Intel Quartus, and hands-on use of FPGA boards.
	PO9	3	Execution of hardware interfacing tasks is often done in pairs or groups, emphasizing collaborative and individual efforts.
	PO10	1	Minimal communication demands; may involve basic reporting or explaining implementation to instructors or peers.
	PO12	3	Hands-on work with FPGA fosters adaptability and ongoing learning of emerging digital hardware platforms and tools.
	PSO1	3	Implementing circuits on FPGA involves design, implementation, testing, and often modeling—all core elements of PSO1.
	PSO2	2	FPGAs are widely used in modern communication systems. This CO involves selecting and interfacing external hardware, supporting PSO2 indirectly.
PCECL308.4	PO1	3	Applying technical knowledge individually and in teams to complete digital circuit tasks reflects sound understanding of core engineering concepts.
	PO2	3	Collaborative problem-solving and task division requires analysis of circuit-related challenges, enhancing group-based learning.
	PO3	3	Team projects often involve planning, designing, and implementing solutions together—directly

			aligning with this PO.
	PO5	3	Teams typically use modern simulation or FPGA tools collaboratively, requiring joint technical engagement.
	PO9	3	This CO directly corresponds to PO9, focusing on functioning effectively in diverse roles, both independently and as a group member.
	PO12	3	Working in teams fosters soft skills like adaptability, communication, and openness to peer learning—critical for lifelong learning.
	PSO1	1	This CO is focused on teamwork and collaboration, not directly on technical aspects like circuit design or signal processing.
	PSO2	1	Similarly, this CO does not involve technology selection or communication systems. It is a **soft skill-oriented** outcome.

CORRELATION Levels: 3- Substantial (High) 2- Moderate (Medium) 1-Slight (Low)

GAPS IN THE SYLLABUS-TO MEET INDUSTRY/PROFESSION REQUIREMENTS

SL NO:	DESCRIPTION	PROPOSED ACTIONS	RELEVANCE WITH POS /PSOS
1	Lack of industry-level HDL project design	Add a **mini-project** on implementing a digital subsystem (e.g., ALU, UART controller, memory interface, or FSM).	PO1, PO2, PO3, PO4, PO5, PO12 PSO1 (3), PSO2 (2)

CONTENT BEYOND THE SYLLABUS/ADVANCED TOPICS/DESIGN

SL NO:	DESCRIPTION	PROPOSED ACTIONS	RELEVANCE WITH POS /PSOS

1	Mini Project: Design of ALU or UART using Verilog	Students design a basic ALU or UART controller using Verilog, simulate, and implement on FPGA.	PO1, PO2, PO3, PO4, PO5, PO12 PSO1 (3), PSO2 (2)
2	Design of a BCD to 7-Segment Decoder	A complete Verilog project implemented on FPGA and connected to physical display hardware.	PO1, PO3, PO5, PO9 PSO1
3	Team-Based HDL Project with Report and Presentation	Collaborative implementation of a design problem, including documentation and demonstration.	PO3, PO9, PO10, PO1 PSO1, PSO2

WEB SOURCE REFERENCES:

SL NO:	DESCRIPTION
1	Nptel Course: Fundamentals of Digital Circuits
2	Nptel Course: System Design through Verilog
3	http://www.electronics-tutorials.ws/logic/logic_1.html
4	https://archive.nptel.ac.in/courses/117/106/117106086/
5	https://archive.nptel.ac.in/courses/106/105/106105185/

DELIVERY TECHNOLOGIES

CLASSROOM WITH BLACK BOARD/WHITE BOARD/SMART BOARD	▯	**ICT TOOLS**	
CLASSROOM WITH LCD PROJECTOR		**ELECTRONIC CLASSROOM**	

INSTRUCTION METHODS

FACE TO FACE INSTRUCTION	Direct		**FLIPPED CLASSROOM**	
	Project-based instruction	▯	**BLENDED LEARNING**	
	Problem-based instruction		**ONLINE COURSES/MOOCs**	
	Technology enhanced learning		**OTHERS (IF ANY)**	
	Experiential learning	▯		
	Participative learning			

CO ASSESSMENT TOOLS-DIRECT

ASSIGNMENTS		**TUTORIALS**		**SERIES EXAMINATIONS**		**UNIVERSITY EXAM**	▯
LAB PRACTICES	▯	**VIVA**	▯	**INTERNAL LAB EXAM**	▯	**REPORT/ DOCUMENT PREPARATION**	▯
PRESENTATION		**EVALUATION BY GUIDE**		**INTERIM EVALUATION**		**FINAL EVALUATION**	

CO ASSESSMENT TOOLS -INDIRECT

ASSESSMENT OF COURSE OUTCOMES (BY COURSE EXIT (END) SURVEY)	▯

ASSESSMENT ITEMS /CLASS SESSIONS/LAB/FIELD/TUTORIAL HOURS FOR EACH COURSE OUTCOMES

CO	ASSESSMENT ITEMS	CLASS SESSIONS	LAB/FIELD/TUTORIAL HOURS
PCECL308.1	CA,IE		24
PCECL308.2	CA,IE		12
PCECL308.3	CA,IE		6
PCECL308.4	CA,IE		42
		TOTAL HOURS OF INSTRUCTION	42

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