St. Thomas College of Engineering & Technology
Vellilode, Sivapuram PO. Mattanur. Kannur District, Kerala
Approved by AICTE New Delhi, Govt. Of Kerala and Affiliated to APJ Abdul Kalam Technological University

COURSE HANDOUT

(B. Tech - Semester 3)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COLLEGE VISION

To be an Institute of repute recognized for excellence in education, innovation, and social contribution.

COLLEGE MISSION

M1: Infrastructural Relevance - Develop, maintain and manage our campus for our stakeholders.
M2: Life-Long Learning - Encourage our stakeholders to participate in lifelong learning through industry and academic interactions.
M3: Social Connect - Organize socially relevant outreach programs for the benefit of humanity.

DEPARTMENT VISION

To produce professionally competent, ethically sound and socially responsible Electronics and Communication Engineers.

DEPARTMENT MISSION

M1: Provide excellent infrastructure and lab facilities for quality education.

M2: Promote industry-academic interactions to keep up with technological advancements.

M3: Develop interpersonal skills and social responsibility among students through project-based and team-based learning.

PROGRAM EDUCATIONAL OBJECTIVES (PEO)

Graduates of B. Tech ECE program after graduation will:

PEO1: Exemplify technical competence in designing, analyzing, testing and fabricating electronic circuits.

PEO2: Acquire leadership qualities, rapport, communication skills in the organization and adapt to changing professional and societal needs.

PEO3: Work effectively as individuals and as team members in multidisciplinary projects

PROGRAM OUTCOMES (POS)

Engineering Graduates will be able to:

PO1 Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2 Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3 Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4 Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5 Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6 The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7 Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8 Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9 Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10 Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11 Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12 Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSO)

PSO1: Define, design, implement, model, and test electronic circuits and systems that perform signal processing functions.

PSO2: Segregate and select appropriate technologies for implementation of a modern communication system.

CONTENTS

COURSE INFORMATION SHEETS OF SEMESTER 3 COURSES

D

PBECT304

LOGIC CIRCUIT DESIGN

COURSE INFORMATION SHEET

PROGRAMME: ECE (UG)	**DEGREE**: BTECH
COURSE: LOGIC CIRCUIT DESIGN	**SEMESTER: III** **L-T-P-R 3:0:0:1 CREDITS**: 4
COURSE CODE: PBECT304 **REGULATION**:2024	**COURSE TYPE**: CORE
COURSE AREA/DOMAIN: DIGITAL ELCTRONICS	**CONTACT HOURS**:6 HRS/WEEK
CORRESPONDING LAB COURSE CODE (IF ANY): PCECL308	**LAB COURSE NAME**: LOGIC CIRCUIT DESIGN LAB

SYLLABUS

MODULE	DETAILS	HOURS
I	**Introduction to digital circuits**: Review of number systems representation conversions, Arithmetic of Binary number systems, Signed and unsigned numbers, BCD. **Boolean algebra**: Theorems, sum of product and product of sum - simplification, canonical forms- min term and max term, Simplification of Boolean expressions - Karnaugh map (upto 4 variables), Implementation of Boolean expressions using universal gates	9
II	**Combinational logic circuits**- Half adder and Full adders, Subtractors, BCD adder, Ripple carry and carry look ahead adders, Decoders, Encoders, Code converters, Comparators, Parity generator, Multiplexers, De-multiplexers, Implementation of Boolean algebra using MUX. Introduction to Verilog HDL – Basic language elements, Basic implementation of logic gates and combinational circuits	9
III	**Sequential Circuits**: SR Latch, Flip flops - SR, JK, Master-Slave JK, D and T Flip flops. Conversion of Flip flops, Excitation table and characteristic equation. Shift registers- SIPO, SISO, PISO, PIPO and Universal shift registers. Ring and Johnsons counters. Design of Asynchronous, Synchronous and Mod N counters.	9

IV	**Finite state machines** - Mealy and Moore models, State graphs, State assignment, State table, State reduction. **Logic Families**: -Electrical characteristics of logic gates (Noise margin, Fanin, Fan-out, Propagation delay, Transition time, Power -delay product) -TTL, ECL, CMOS. Circuit description and working of TTL and CMOS inverter, CMOS NAND and CMOS NOR gates.	9
Total hours		**36**

TEXT BOOKS/REFERENCE BOOKS:

T/R	BOOK TITLE/AUTHORS/PUBLICATION
T1	Digital Fundamentals, Thomas L. Floyd Pearson Education 11th Edition, 2017
T2	Fundamentals of Digital Logic with Verilog Design Stephen Brown McGraw Hill Education 2 nd Edition
R1	Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog M Morris Mano, Michael D. Ciletti Pearson India 6 th Edition, 2018
R2	Fundamentals of Digital Circuits A. Ananthakumar PHI 4 th Edition, 2016
R3	Introduction to Logic Circuits & Logic Design with Verilog Brock J. LaMeres Springer 2 nd Edition, 2019
R4	Digital Design Verilog HDL and Fundamentals Joseph Cavanagh CRC Press 1 st Edition, 2008
R5	Digital Circuits and Systems D.V. Hall Tata McGraw Hill 1989

COURSE PREREQUISITES:

COURSE CODE	COURSE NAME	DESCRIPTION	SEMESTER
GYEST104	INTRODUCTION TO ELECTRICAL & ELECTRONICS ENGINEERING	It provides the foundational knowledge of electrical and electronic circuits, components, and systems that are essential for understanding and working with digital technologies.	I/II

COURSE OBJECTIVES:

1	To understand the number systems in digital systems
2	To introduce the basic postulates of Boolean algebra, digital logic gates and Boolean expressions
3	To design and implement combinational and sequential circuits
4	To design and implement digital circuits using Hardware Descriptive Language like Verilog on FPGA

COURSE OUTCOMES:

After the completion of the course, the student will be able to

COs / CO-PO/PSO MAPPING. /BLOOM'S TAXONOMY LEVEL	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
PBECT304.1	Apply the knowledge of digital representation of information and Boolean algebra to deduce optimal digital circuits.													
	3	**3**	**2**	**2**								**3**	**3**	**2**
	APPLY													
PBECT304.2	Design and implement combinational logic circuits, sequential logic circuits and finite state machines													
	3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**			**3**	**3**	**2**
	EVALUATE													
PBECT304.3	Design and implement digital circuits on FPGA using hardware description language (HDL)													
	3	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**2**
	EVALUATE													
PBECT304.4	Outline the performance of logic families with Respect to different parameters													
	3		**2**									**3**	**2**	**2**
	UNDERSTAND													
MAPPING AVERAGE	**3.00**	**3.00**	**2.50**	**2.67**	**3.00**	**3.00**	**3.00**	**3.00**	**3.00**	**3**	**3**	**3**	**2.75**	**2**

JUSTIFICATION FOR CO-PO/PSO MAPPING:

CO	PO/PSO	MAPPING LEVEL	JUSTIFICATION
PBECT304.1	PO1	3	Students get core engineering fundamentals—specifically, digital logic and Boolean algebra. These are foundational concepts in electronics and communication engineering. Applying these concepts to design optimal circuits directly reflects strong use of engineering principles
	PO2	3	Students are required to analyse digital problems such as circuit optimization, logic simplification, and binary representation of information. This involves critical analysis and decomposition of the problem into solvable components
	PO3	2	Designing optimal digital circuits involves selecting suitable logic components and optimizing the design using Karnaugh Maps or Boolean expressions.
	PO4	2	Students often need to explore different design alternatives and test circuit behaviour through simulation or analysis to achieve optimization. This involves investigation skills
	PO12	3	The field of digital design is constantly evolving. The ability to continuously update knowledge on digital representation techniques and logic optimization is essential.
	PSO1	3	This CO focuses on applying Boolean algebra and digital principles to design and optimize digital circuits. These are foundational skills for building electronic systems, especially those involved in signal processing such as encoders, decoders, multiplexers, etc. Students define logic requirements, design

			circuits, model them using Boolean expressions or HDL, and test their functionality
	PSO2	2	While the primary focus of the CO is on logic design, these skills indirectly support communication system design, where digital circuits like modulators/demodulators, encoders/decoders, or data converters are integral. The knowledge gained here enables students to choose suitable logic components for communication subsystems
PBECT304.2	PO1	3	Designing digital circuits requires in-depth understanding of Boolean algebra, logic gates, and electronics principles that strongly apply engineering knowledge.
	PO2	3	Students must analyze circuit specifications, truth tables, and timing requirements before design, which demonstrates thorough problem analysis.
	PO3	3	Students will gain knowledge in designing and developing solutions in the form of logic circuits and FSMs.
	PO4	3	Simulation and testing of logic and sequential circuits require problem-solving, debugging, and verifying behavior under various inputs.
	PO5	3	Students use simulation tools (e.g., ModelSim, Xilinx) for design and testing, satisfying modern engineering tool usage.
	PO6	3	Logic circuits are used in real-time applications and implementing them improves understanding of socially relevant designs.
	PO7	3	Efficient circuit design reduces power usage and hardware complexity, supporting sustainability

			goals.
	PO8	3	Encourages ethical design, such as avoiding plagiarism in HDL code and responsibly using licensed tools and open-source IPs.
	PO9	3	Students typically perform lab and project work in teams, encouraging team collaboration and leadership.
	PO12	3	As digital technologies evolve, learning modern circuit design tools and methods fosters lifelong learning.
	PSO1	3	This involves complete digital system development (FSMs, sequential/combinational logic on circuit definition, design, and testing
	PSO2	2	Understanding and implementing control and timing logic is relevant to communication subsystems.
PBECT304.3	PO1	3	Students apply digital electronics concepts, logic design, and HDL coding—core technical knowledge areas.
	PO2	3	Requires analyzing functional requirements of digital circuits and converting them into HDL models.
	PO3	3	Involves complete design life cycle—writing HDL, simulating, synthesizing, and implementing on FPGA.
	PO4	3	Testing and debugging HDL designs on FPGA demands investigative skills for timing, logic errors, and optimization.
	PO5	3	Students use FPGA tools such as Vivado, Quartus, ModelSim, etc.
	PO6	3	HDL-based circuit design has applications in areas like medical electronics, automotive, and communication—helping address real-world

			needs.
	PO7	3	Efficient FPGA design reduces power consumption and hardware usage—supporting sustainability goals.
	PO8	3	Students must follow ethical practices in IP core usage, licensing, and responsible coding.
	PO9	3	Design projects are often collaborative, enhancing teamwork and task delegation.
	PO10	3	Students document HDL designs and communicate technical details through simulation results and project reports.
	PO11	3	Designing on FPGA within resource constraints builds project planning, budgeting and time management skills.
	PO12	3	Digital design tools and HDLs continuously evolve, making self-learning of tools and techniques essential.
	PSO1	3	Students design, test, and implement digital circuits using HDL on hardware platforms.
	PSO2	2	HDL is widely used in communication systems (e.g., protocol design, digital filters, encoding/decoding). Students learn how to choose appropriate HDL modules and platforms.
PBECT304.4	PO1	3	Understanding logic families (TTL, CMOS, ECL, etc.) and comparing parameters like speed, power, noise margin, fan-out relies on core electronics engineering concepts
	PO3	2	Involving design, knowledge of logic family parameters supports design decisions, such as selecting suitable logic types for specific applications.
	PO12	3	Logic families evolve (e.g., low-power CMOS, BiCMOS), and staying updated on new families

			or improved versions is key for continuing professional development.
	PSO1	2	Understanding the electrical characteristics of logic families is essential for reliable design and testing of digital circuits, impacting parameters like propagation delay and loading.
	PSO2	2	Selecting logic families based on speed or power requirements influences digital communication hardware design.

CORRELATION Levels: 3- Substantial (High) 2- Moderate (Medium) 1-Slight (Low)

GAPS IN THE SYLLABUS-TO MEET INDUSTRY/PROFESSION REQUIREMENTS

SL NO:	DESCRIPTION	PROPOSED ACTIONS	RELEVANCE WITH POs /PSOs
1	Familiarization of System Design through HDL	Expert Talk /Hands on Session /Attend MOOC Course(nptel)/Laboratory Session	PO1, PO2, PO3, PO4, PO5, PO9, PO10, PO12, PSO1(3), PSO2(2)

CONTENT BEYOND THE SYLLABUS/ADVANCED TOPICS/DESIGN

SL NO:	DESCRIPTION	PROPOSED ACTIONS	RELEVANCE WITH POS /PSOS
1	Implementation of digital circuit designs on FPGA	Design Activities (Project/Assignment Ideas)	PO1, PO2, PO3, PO4, PO5, PO9, PO12.PSO1 (3), PSO2 (2)
2	Exposure to latest trends in IC Design	Seminar/Expert Talk	PO1, PO2, PO3, PO4, PO5, PO12 PSO1 (3), PSO2 (2)

WEB SOURCE REFERENCES:

SL NO:	DESCRIPTION
1	Nptel Course: Fundamentals of Digital Circuits
2	Nptel Course: System Design through Verilog
3	http://www.electronics-tutorials.ws/logic/logic_1.html
4	https://archive.nptel.ac.in/courses/117/106/117106086/
5	https://archive.nptel.ac.in/courses/106/105/106105185/

DELIVERY TECHNOLOGIES

CLASSROOM WITH BLACK BOARD/WHITE BOARD/SMART BOARD	▯	**ICT TOOLS**	▯
CLASSROOM WITH LCD PROJECTOR	▯	**ELECTRONIC CLASSROOM**	

INSTRUCTION METHODS

FACE TO FACE INSTRUCTION	Direct	▯	**FLIPPED CLASSROOM**	
	Project-based instruction	▯	**BLENDED LEARNING**	
	Problem-based instruction		**ONLINE COURSES/MOOCs**	
	Technology enhanced learning	▯	**OTHERS (IF ANY)**	
	Experiential learning			
	Participative learning			

CO ASSESSMENT TOOLS-DIRECT

ASSIGNMENTS		**TUTORIALS**		**SERIES EXAMINATIONS**	▯	**UNIVERSITY EXAM**	▯
LAB PRACTICES		**VIVA**		**INTERNAL LAB EXAM**		**REPORT/ DOCUMENT PREPARATION**	▯
PRESENTATION	▯	**EVALUATION BY GUIDE**		**INTERIM EVALUATION**	▯	**FINAL EVALUATION**	▯

CO ASSESSMENT TOOLS -INDIRECT

ASSESSMENT OF COURSE OUTCOMES (BY COURSE EXIT (END) SURVEY)	▯

ASSESSMENT ITEMS /CLASS SESSIONS/LAB/FIELD/TUTORIAL HOURS FOR EACH COURSE OUTCOMES

CO	ASSESSMENT ITEMS	CLASS SESSIONS	LAB/FIELD/TUTORIAL HOURS
PBECT304.1	S1, PBL	14	

			16(PBL)
PBECT304.2	S2, S3, PBL	30	
PBECT304.3	S2, PBL	4	
PBECT304.4	S3,PBL	5	
		TOTAL HOURS OF INSTRUCTION	53 +16(PBL)

Prepared by:
Dr Anetha Mary Soman

Approved by HOD:
Prof.Nithin C